SIR ARTHUR LEWIS COMMUNITY COLLEGE

ENGINEERING AND THE CIRCULAR ECONOMY

ACADEMIC YEAR (2024/2025) – SEMESTER TWO

END OF SEMESTER EXAMINATION

LECTURER(S)	**:**	**Mr Kendall Numa**
PROGRAMME TITLE	**:**	**Computer Systems Engineering** **Electronics Engineering**
COURSE TITLE	**:**	**Digital Principles & Technology**
COURSE CODE	**:**	**ELE211**
LEVEL	**:**	**Associate Degree/ Year Twos**
PAPER	**:**	**One**
DATE	**:**	**Tuesday, 6th May 2025**
COMMENCEMENT TIME	**:**	**9:00a.m.**
DURATION	**:**	**TWO (2) HOURS**
INVIGILATOR(S)	**:**	**K. Emmanuel (chief),** A. Cadasse-Paul, A Sanchez Rojo, C. Fevriere & P. Jn Francois
ROOM(S)	**:**	**LFT-1R-05**

GENERAL INFORMATION AND INSTRUCTIONS

- This paper consist of Two (2) Sections.
- **Section A** consist of eight (8) questions. You are required to **answer ALL questions**.
- **Section B** consist of three (3) questions. You are required to **answer ANY TWO (2) questions.**
- All questions are to be attempted on the foolscap paper provided.
- The number in the brackets "[]" next to each question are the marks allocated.
- Students must sign **IN** and **OUT** on the examination class list.
- Students must **not** write their names on their answer sheets, only their ID number
- Please number your responses accurately.

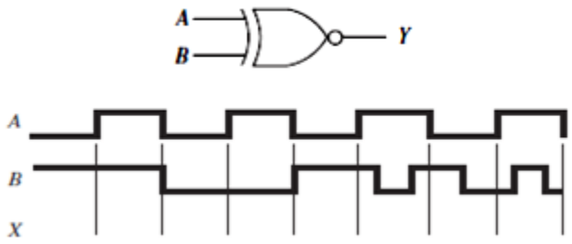
DO NOT TURN THIS COVER SHEET UNTIL
YOU ARE TOLD TO DO SO!!!

SECTION A

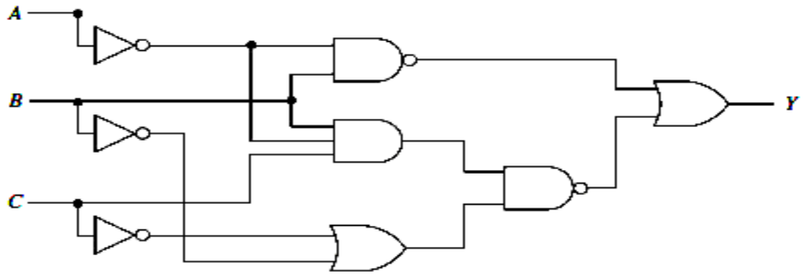
Answer ALL questions.

1. State the function of the following gates: AND, NOR and XOR [6]

2. Determine the output waveform for the diagrams shown below [6]



3. Determine the **Boolean Expression** for the following combinational logic circuit. [5]



4. Draw the **truth table** for the circuit diagram shown in question three (3) above. [6]

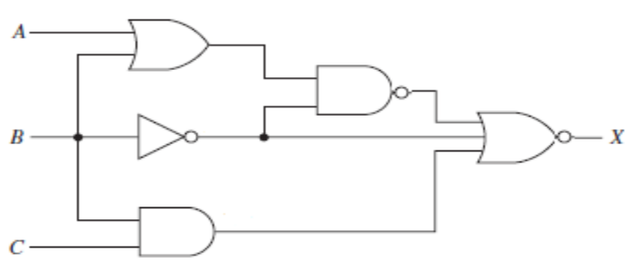
5. Draw the logic circuit for the following Boolean expression: [4]

$$Y = \overline{AB\bar{C} + D} + \overline{A\bar{B} + B\bar{C}}$$

6. Simplify the following Boolean expression using the rules and theorems of Boolean algebra:
$Y = \overline{AB\bar{C} + D} + \overline{A\bar{B} + B\bar{C}}$ [4]

7. Use a Karnaugh map to simplify the following boolean expression: [8]
$X = \bar{B}(C\bar{D} + \bar{A}D) + \bar{B}\bar{C}(A + \bar{A}\bar{D})$

8. Redraw the following circuit using NOR gates only [11]



Total [50 Marks]

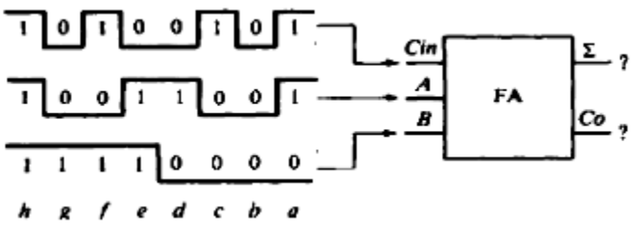
SECTION B

Answer any two (2) questions.

Question One

(A) Draw the block diagram, truth table and circuit diagram for a half adder. [6]

(B) Draw the output waveforms for the diagram shown below:

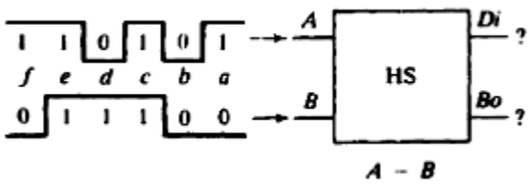


[4]

(C) Draw a 4 bit parallel adder using one half adder and three full adders. [3]

(D) Draw the circuit diagram for a full subtractor. [4]

(E) Draw the output waveforms for the diagram shown below:

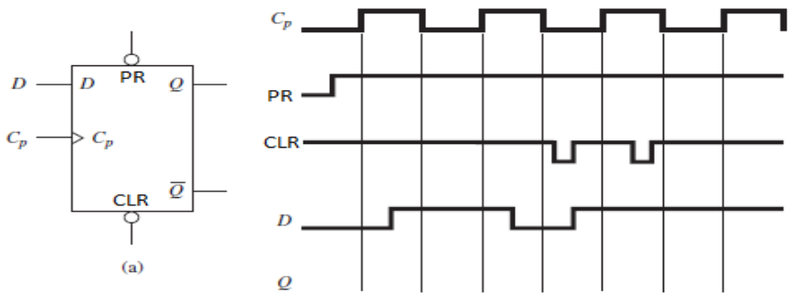


[3]

Question Two

(A) Draw logic circuits diagrams of the SR latch using NAND gates only and NOR gates only. [4]

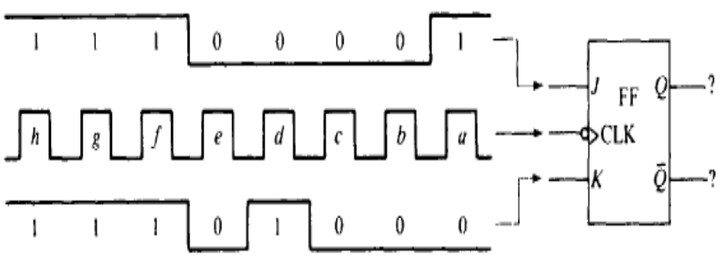
(B) Draw the characteristics table for the device and the Q output for the diagram shown below.



[6]

(C) Draw the Q and $\bar{Q}$ outputs for the diagram shown below.

a.

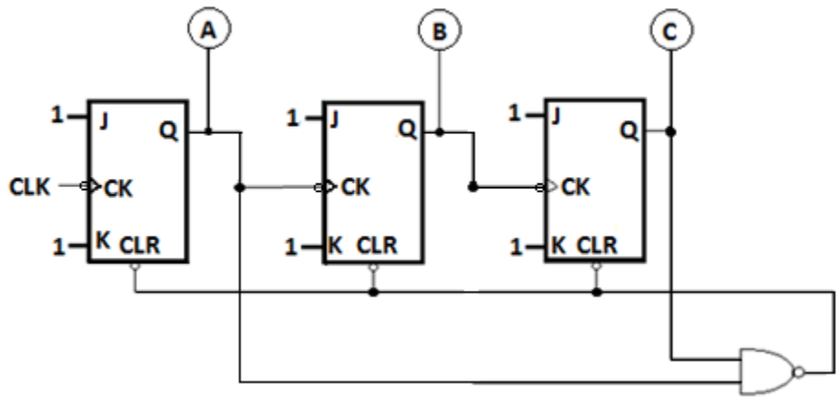


[4]

(D) Define the following terms: sequential logic circuit, asynchronous sequential logic circuit, synchronous sequential logic circuit [6]

Question Three

(A) Produce the output waveforms for the next eight (8) clock cycles. The initial state of outputs CBA is 011.



[4]

(B) Give the four main characteristics of the device shown above. [4]

(C) Produce a diagram of a three-bit register connected as SIPO. [3]

(D) A four bit Johnson counter has the initial conditions 0101. Produce the next state table (truth table), for the next five clock cycles. [5]

(E) Draw the circuit diagram for a 4-bit synchronous counter. [4]

Total [40 Marks]

END OF EXAMINATION!!